This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

1. (Currently Amended) A strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) transistor device having gate stress engineering with SiGe and/or Si:C, comprising:

a substrate of either bulk silicon (Si) or silicon on insulator (SOI), and a gate dielectric layer over the substrate;

a stacked gate structure of SiGe and/or Si:C to produce stresses by the structures of SSi(strained Si)/SiGe or SSi/Si:C in the stacked gate structure and having a first stressed film layer of large grain size Si or SiGe ~~over~~ formed on top the gate dielectric layer, a second stressed film layer of strained SiGe or strained Si:C ~~over~~ formed on top the first stressed film layer, and a semiconductor or conductor ~~such as p(poly) Si over~~ layer formed on top the second stressed film layer.

2. (Original) The device of claim 1, wherein stress is produced in the stacked gate structure by different semiconductor materials and/or by different percentages of semiconductor materials.

3. (Original) The device of claim 1, fabricated on a chip having both nFET devices and pFET devices, and wherein the nFET devices and pFET devices have different stresses.

4. (Original) The device of claim 3, wherein the stacked gate structure of the nFET devices comprises the second stressed film layer of strained SiGe over the first stressed film layer of single crystal silicon, and the stacked gate structure of the pFET devices comprises the second stressed film layer of strained Si:C over the first stressed film layer of single crystal silicon.

5. (Original) The device of claim 3, wherein the stacked gate structure of the nFET devices comprises the second stressed film layer of strained $Si_{1-y}Ge_y$ over the first stressed

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film layer of strained $Si_{1-x}Ge_x$, and the stacked gate structure of the pFET devices comprises the second stressed film layer of strained $Si_{1-z}Ge_z$ over the first stressed film layer of strained $Si_{1-x}Ge_x$, wherein y>x and z<x to produce different stresses.

6. (Original) The device of claim 5, wherein the value of x is selected to adjust the pFET Vt (threshold voltage).

7. (Original) The device of claim 5, wherein the $Si_{1-x}Ge_x$ is a seed layer for parts of the gate above the $Si_{1-x}Ge_x$ layer, and the $Si_{1-x}Ge_x$ layer is strained after selective epitaxial growth.

8. (Original) The device of claim 3, wherein the stacked gate structure of the nFET devices comprises the second stressed film layer of strained $Si_{1-y}Ge_y$ over the first stressed film layer of strained $Si_{1-xn}Ge_{xn}$, and the stacked gate structure of the pFET devices comprises the second stressed film layer of strained $Si_{1-z}Ge_z$ over the first stressed film layer of strained $Si_{1-xp}Ge_{xp}$, wherein y>xn and z<xp, to produce stresses.

9. (Original) The device of claim 8, wherein the $Si_{1-xn}Ge_{xn}$ is a seed layer for parts of the gate above the $Si_{1-xn}Ge_{xn}$ seed layer and the $Si_{1-xn}Ge_{xn}$ seed layer is strained after selective epitaxial growth, and the $Si_{1-xp}Ge_{xp}$ is a seed layer for parts of the gate above the $Si_{1-xp}Ge_{xp}$ seed layer and the $Si_{1-xp}Ge_{xp}$ seed layer is strained after selective epitaxial growth.

10. (Original) The device of claim 3, wherein the stacked gate structure of the nFET devices comprises the second stressed film layer of strained $Si_{1-y}Ge_y$ over the first stressed film layer of strained $Si_{1-x}Ge_x$, and the stacked gate structure of the pFET devices comprises the second stressed film layer of strained Si:C over the first stressed film layer of strained $Si_{1-x}Ge_x$, wherein y>x and z<x, to produce different stresses.

11. (Original) The device of claim 1, fabricated in an integrated circuit comprising both nFET devices and pFET devices having said stacked gate structure.

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12. (Original) The device of claim 1, fabricated in an integrated circuit comprising nFET devices having said stacked gate structure.

13. (Original) The device of claim 1, fabricated in an integrated circuit comprising pFET devices having said stacked gate structure.

14. (Withdrawn) A process of fabricating a strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) device having gate stress engineering with SiGe and/or Si:C, comprising:

depositing a(amorphous)-Si or poly-Si over a gate oxide on a bulk Si or SOI substrate, and annealing to obtain poly-Si with a large grain size;

depositing poly-SiGe to form a stacked-gate layer;

performing a replacement gate process;

depositing oxide, followed by CMP (chemical mechanical polishing), stopping on the top of gates, and depositing a thin nitride layer;

covering and patterning the pFETs with photoresist,

processing the nFETs by etching the nitride and selectively etching the p-SiGe gate for the nFETs, removing the photoresist, performing selective epitaxial growth of strained single crystal-SiGe, filling poly-Si in the nFETs and CMP stopping on the oxide;

depositing a thin nitride layer and photoresist and repeating the previous processing step, but this time covering the nFETs and processing the pFETs.

15. (Withdrawn) The process of claim 14, including after the step of annealing, oxidizing and etching the large grain poly-Si layer to attain a selected thickness.

16. (Withdrawn) A process of fabricating a strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) device having gate stress engineering with SiGe and/or Si:C, comprising:

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depositing a(amorphous)-Si or poly-Si over a gate oxide on a bulk Si or SOI substrate, and annealing to obtain poly-Si with a large grain size;

depositing poly-SiGe to form a stacked-gate layer;

performing a replacement gate process;

depositing oxide, followed by CMP (chemical mechanical polishing), stopping on the top of gates, and depositing a thin nitride layer;

covering and patterning the nFETs with photoresist,

processing the pFETs by etching the nitride and selectively etching the p-SiGe gate for the pFETs, removing the photoresist, performing selective epitaxial growth of strained single crystal-SiGe, filling poly-Si in the pFETs and CMP stopping on the oxide;

depositing a thin nitride layer and photoresist and repeating the previous processing step, but this time covering the pFETs and processing the nFETs.

17. (Withdrawn) The process of claim 16, including after the step of annealing, oxidizing and etching the large grain poly-Si layer to attain a selected thickness.

18. (Withdrawn) A process of fabricating a strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) device having gate stress engineering with SiGe and/or Si:C, comprising:

depositing relaxed large grain poly-$Si_{1-x}Ge_x$ over a gate oxide on a bulk Si or SOI substrate, and annealing to obtain poly-$Si_{1-x}Ge_x$ with a large grain size;

depositing poly-Si to form a stacked-gate layer;

performing a replacement gate process;

depositing oxide, followed by CMP (chemical mechanical polishing), stopping on the top of gates, and depositing a thin nitride layer;

covering and patterning the pFETs with photoresist,

processing the nFETs by etching the nitride and selectively etching the p-Si gate for the nFETs, removing the photoresist, performing selective epitaxial growth of strained single crystal-$Si_{1-y}Ge_y$ ($y>x$), filling poly-Si in the nFETs and CMP stopping on the oxide;

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depositing a thin nitride layer and photoresist and repeating the previous processing step, but this time covering the nFETs and processing the pFETs, growing$Si_{1-z}Ge_z$ ($z<x$).

19. (Withdrawn) A process of fabricating a strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) device having gate stress engineering with SiGe and/or Si:C, comprising:

depositing relaxed large grain poly-$Si_{1-x}Ge_x$ over a gate oxide on a bulk Si or SOI substrate, and annealing to obtain poly-$Si_{1-x}Ge_x$ with a large grain size;

depositing poly-Si to form a stacked-gate layer;

performing a replacement gate process;

depositing oxide, followed by CMP (chemical mechanical polishing), stopping on the top of gates, and depositing a thin nitride layer;

covering and patterning the nFETs with photoresist,

processing the pFETs by etching the nitride and selectively etching the p-Si gate for the pFETs, removing the photoresist, performing selective epitaxial growth of strained single crystal-$Si_{1-y}Ge_y$ ($y>x$), filling poly-Si in the pFETs and CMP stopping on the oxide;

depositing a thin nitride layer and photoresist and repeating the previous processing step, but this time covering the pFETs and processing the nFETs, growing$Si_{1-z}Ge_z$ ($z<x$).

20. (Withdrawn) A process of fabricating a strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) device having gate stress engineering with SiGe and/or Si:C , comprising:

forming a stacked structure of SiGe and/or Si:C having stresses at the interfaces of SSi(strained Si)/SiGe or SSi/Si:C in the stacked structure and having a first stressed film layer of large grain size Si or SiGe over the gate dielectric layer, a second stressed film layer of strained SiGe or strained Si:C over the first stressed film layer, and a semiconductor or conductor such as p-Si over the second stressed film layer; and

patterning the stacked structure to form a patterned stacked gate structure.

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21. (Withdrawn) A process of fabricating a strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) device having gate stress engineering with SiGe and/or Si:C, comprising:

forming a bonded handle wafer with two single crystalline Si layers having a respective bonded oxide/Si interface and a thermal oxide/Si interface;

depositing p(poly)-SiGe on the bonded handle wafer to form a stacked-gate layer;

performing a replacement gate process;

depositing oxide, followed by CMP (chemical mechanical polishing), stopping on top of gates, and depositing a thin nitride layer;

covering and patterning the pFETs with photoresist,

processing the nFETs by etching the nitride and selectively etching the p-SiGe gate for the nFETs, removing the photoresist, performing selective epitaxial growth of strained single crystal-SiGe, filling poly-Si in the nFETs and CMP stopping on the oxide;

depositing a thin nitride layer and photoresist and repeating the previous processing step, but this time covering the nFETs and processing the pFETs.

22. (Withdrawn) A process of fabricating a strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) device having gate stress engineering with SiGe and/or Si:C, comprising:

forming a bonded handle wafer with two single crystalline Si layers having a respective bonded oxide/Si interface and a thermal oxide/Si interface;

depositing p(poly)-SiGe on the bonded handle wafer to form a stacked-gate layer;

performing a replacement gate process;

depositing oxide, followed by CMP (chemical mechanical polishing), stopping on top of gates, and depositing a thin nitride layer;

covering and patterning the nFETs with photoresist,

processing the pFETs by etching the nitride and selectively etching the p-SiGe gate for the pFETs, removing the photoresist, performing selective epitaxial growth of strained single crystal-SiGe, filling poly-Si in the pFETs and CMP stopping on the oxide;

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depositing a thin nitride layer and photoresist and repeating the previous processing step, but this time covering the pFETs and processing the nFETs.

23. (Withdrawn) A process of fabricating a strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) device having gate stress engineering with SiGe and/or Si:C , in a process to make the structure with the double single crystal layers and using regrowth of single crystal from an a-Si layer, starting the a seeds near the gates, comprising:

forming a gate oxide layer on a single crystal Si substrate, and then depositing a thin layer of a(amorphous)-Si:

depositing and patterning photoresist, etching the a-Si, and etching the gate oxide;

removing the photoresist and depositing a-Si;

patterning the photoresist to covers both nFET regions and pFET regions, and etching the a-Si down to the gate oxide to isolate the nFET regions and the pFET regions for regrowth of crystal Si;

annealing the structure to recrystalize the a-Si layer to form single crystal Si.

24. (Withdrawn) A process of fabricating a strained bulk silicon or SOI (silicon on insulator) MOS (metal oxide semiconductor) device having gate stress engineering with SiGe and/or Si:C, comprising:

depositing a(amorphous)-Si or poly-Si over a gate oxide on a bulk Si or SOI substrate, and annealing to obtain poly-Si with a large grain size;

depositing poly-SiGe to form a stacked-gate layer;

performing a replacement gate process;

depositing oxide, followed by CMP (chemical mechanical polishing), stopping on the top of gates, and depositing a thin nitride layer;

covering and patterning nFETs with photoresist;

processing pFETs by implantating carbon into pFET gates, and annealing to produce tensile stress in implanted areas in the pFET gates.

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